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| 10/648,510 | 08/27/2003 | Fumitaka Arai | 241987US2S | 4228 |

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| EXAMINER |
|---|
| HO, TU TU V |

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|---|---|
| 2818 | |

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/648,510 | ARAI ET AL. | |
| | Examiner | Art Unit | |
| | Tu-Tu Ho | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3 and 5-40* is/are pending in the application.

4a) Of the above claim(s) *8-23 and 25-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,24 and 40* is/are rejected.

7)☒ Claim(s) *6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 08/16/2005 has been entered.

### *Allowable Subject Matter*

2. The indicated allowability of claims **1-3, 5-7, 28-39, 24, and 40** is withdrawn in view of the newly discovered reference(s) to Horiguchi et al. (U.S. Patent Application PUblication 20010002712), Chang et al. (U.S. Patent 6,291,855), and Wang et al. (U.S. Patent 6,617,639). Rejections based on the newly cited reference(s) follow.

### *Election/ Restriction*

3. Claims 1-3 and 5-40 are pending. The claims have been restricted into two species, and Applicant has elected Species I, which readable on claims 1-7, 24, and 40. Claims 8-23 and 25-39 have been withdrawn.

***Claim Objections***

4. Claim 3 is objected to because of the following informalities: Claim 3 recites "wherein the inter-gate insulating film includes first and second portions, the first portion contacts the floating gate, the second portion contacts the lower surface of the first or second control gate" which has been recited in claim 1, from which claim 3 depends. Applicant is required to cancel to limitation because it fails to further the limitations of a previous claim.

5. Claim 7 is objected to because of the following informalities: the dependency of claim 7 is claim 4, which has been canceled. Perhaps the dependency of claim 7 is claim 6, since claim 7 recites a third trench, which may not require, but logically should have, first and second trenches, which are recited in claim 6.

***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. **Claims 1, 5, 24, and 40** are rejected under 35 U.S.C. §103(a) as being unpatentable over Horiguchi et al. U.S. Patent Application Publication 20010002712 (the '712 reference) in view of Wang et al. U.S. Patent 6,617,639.

The '712 reference discloses a nonvolatile semiconductor memory device as claimed including an inter-gate insulating film having a first portion but fails to teach that the first portion is a stacked film including a silicon nitride film.

Specifically, referring to **claim 1**, the reference discloses a nonvolatile semiconductor memory device comprising:

a floating gate (5, Fig. 6B, paragraph [0109]) formed on a semiconductor substrate (1) via a gate insulating film (4);

diffused layers (21,22), as sources or drain regions, which are positioned on opposite sides of the floating gate and which are formed in the semiconductor substrate;

first and second control gates (11) which are formed on the opposite sides of the floating gate and which drive the floating gate; and

an inter-gate insulating film (10A/10B) which insulates the first and second control gates (11) from the floating gate (5) and diffused layers (21,22),

wherein the inter-gate insulating film (10A/10B) includes first and second portions (10A/10B), the first portion (10A) contacts the floating gate, the second portion (10B) contacts the lower surface of the first or second control gate, the first portion is an insulating film, and the second portion (10B) is a single layer of a silicon oxide film (paragraph [0116], "thermal oxidation" of silicon).

However, as noted, the reference teaches that the first portion of the inter-gate insulating film, which first portion insulates the control gate from the floating gate, is an insulating film instead of a stacked film including a silicon nitride film as claimed.

Wang, in also disclosing a nonvolatile semiconductor memory device including a floating gate, a control gate and an inter-gate insulating film insulating the control gate from the floating gate, teaches that the inter-gate insulating film is a stacked film including a silicon nitride film

("ONO"), instead of an insulating film of silicon oxide, to improve the performance of the nonvolatile semiconductor memory device (column 2, lines 10-15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the reference's device such that the first portion (10A) of the inter-gate insulating film, which first portion insulates the control gate from the floating gate, is a stacked film including a silicon nitride film. One would have been motivated to make such a change in view of the teachings in Wang that such a modification results in a better device.

Referring to **claim 24**, and using the same reference characters, interpretations, and citations as detailed above for claim 1 where applicable, the reference discloses a nonvolatile semiconductor memory device comprising:

a floating gate formed above a semiconductor substrate;

first and second control gates which are formed on opposite sides of the floating gate and which are insulated from the floating gate and semiconductor substrate;

a first capacitance (no number, defined by a conductor/insulator/conductor structure of the semiconducting semiconductor substrate/insulating tunneling gate insulator/floating gate) between the semiconductor substrate and floating gate;

a second capacitance (no number, defined by a conductor/insulator/conductor structure) between the first control gate and floating gate;

a third capacitance (no number, defined by a conductor/insulator/conductor structure) between the second control gate and floating gate;

a fourth capacitance (no number, defined by a conductor/insulator/conductor structure) between the first control gate and semiconductor substrate; and

a fifth capacitance (no number, defined by a conductor/insulator/conductor structure) between the second control gate and semiconductor substrate,

wherein the inter-gate insulating film includes first and second portions, the first portion contacts the floating gate, the second portion contacts the lower surface of the first or second control gate, the first portion is an insulating film, and the second portion is a single layer of a silicon oxide film.

However, as noted, the reference teaches that the first portion of the inter-gate insulating film, which first portion insulates the control gate from the floating gate, is an insulating film instead of a stacked film including a silicon nitride film as claimed.

Wang, in also disclosing a nonvolatile semiconductor memory device including a floating gate, a control gate and an inter-gate insulating film insulating the control gate from the floating gate, teaches that the inter-gate insulating film is a stacked film including a silicon nitride film ("ONO"), instead of an insulating film of silicon oxide, to improve the performance of the nonvolatile semiconductor memory device (column 2, lines 10-15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the reference's device such that the first portion (10A) of the inter-gate insulating film, which first portion insulates the control gate from the floating gate, is a stacked film including a silicon nitride film. One would have been motivated to make such a change in view of the teachings in Wang that such a modification results in a better device.

Referring to **claims 40 and 5**, and using the same reference characters, interpretations, and citations as detailed above for claim 1 where applicable, the reference discloses a nonvolatile semiconductor memory device comprising:

a floating gate formed on a semiconductor substrate via a gate insulating film;

diffused layers, as sources or drain regions, which are positioned on opposite sides of the floating gate and which are formed in the semiconductor substrate;

first and second control gates which are formed on the opposite sides of the floating gate and which drive the floating gate; and

an inter-gate insulating film which insulates the first and second control gates from the floating gate and diffused layers,

wherein the inter-gate insulating film includes first and second portions, the first portion contacts the floating gate, the second portion contacts the lower surface of the first or second control gate, the first portion is an insulating film, and the second portion is a single layer of a silicon oxide.

However, as noted, the reference teaches that the first portion of the inter-gate insulating film, which first portion insulates the control gate from the floating gate, is an insulating film instead of a single layer or a stacked film containing aluminum oxide as claimed.

Wang, in also disclosing a nonvolatile semiconductor memory device including a floating gate, a control gate and an inter-gate insulating film insulating the control gate from the floating gate, teaches that the inter-gate insulating film is a stacked film containing aluminum oxide, instead of an insulating film of silicon oxide or instead of a traditional stacked ONO, to further improve the performance and scaling down of the nonvolatile semiconductor memory device (column 3, lines 6-25, for motivation; column 4, last paragraph for definition of "high-K dielectric material"; and column 6, Table 1, for a list of high-K dielectric materials).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the reference's device such that the first portion (10A) of the inter-gate insulating film, which first portion insulates the control gate from the floating gate, is a stacked film containing aluminum oxide, which meets the claimed Markush limitation a single layer or a stacked film containing aluminum oxide. One would have been motivated to make such a change in view of the teachings in Wang that such a modification results in a better device.

7. **Claims 1-3, 5, 24, and 40** are rejected under 35 U.S.C. §103(a) as being unpatentable over Chang et al. U.S. Patent 6,291,855 (the '855 reference) in view of Wang et al. U.S. Patent 6,617,639.

The '855 reference discloses a nonvolatile semiconductor memory device as claimed including an inter-gate insulating film having a first portion but fails to teach that the first portion is a stacked film including a silicon nitride film.

Specifically, referring to **claim 1**, the reference discloses a nonvolatile semiconductor memory device comprising:

a floating gate (FG, Fig. 5, column 4, last paragraph) formed on a semiconductor substrate (100) via a gate insulating film (105);

diffused layers (source/drain regions SD), as sources or drain regions, which are positioned on opposite sides of the floating gate and which are formed in the semiconductor substrate;

first and second control gates (103) which are formed on the opposite sides of the floating gate and which drive the floating gate; and

an inter-gate insulating film (105a/102) which insulates the first and second control gates (CG) from the floating gate (FG) and diffused layers (SD),

wherein the inter-gate insulating film (105a/102) includes first and second portions (105a/102), the first portion (105a) contacts the floating gate, the second portion (102) contacts the lower surface of the first or second control gate, the first portion is an insulating film, and the second portion (102) is a single layer of a silicon oxide film (column 5, lines 35-40, "thermal oxide" of silicon).

However, as noted, the reference teaches that the first portion of the inter-gate insulating film, which first portion insulates the control gate from the floating gate, is an insulating film instead of a stacked film including a silicon nitride film as claimed.

Wang, in also disclosing a nonvolatile semiconductor memory device including a floating gate, a control gate and an inter-gate insulating film insulating the control gate from the floating gate, teaches that the inter-gate insulating film is a stacked film including a silicon nitride film ("ONO"), instead of an insulating film of silicon oxide, to improve the performance of the nonvolatile semiconductor memory device (column 2, lines 10-15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the reference's device such that the first portion (105a) of the inter-gate insulating film, which first portion insulates the control gate from the floating gate, is a stacked film including a silicon nitride film. One would have been motivated to make such a change in view of the teachings in Wang that such a modification results in a better device.

Referring to **claim 24**, and using the same reference characters, interpretations, and citations as detailed above for claim 1 where applicable, the reference discloses a nonvolatile semiconductor memory device comprising:

a floating gate formed above a semiconductor substrate;

first and second control gates which are formed on opposite sides of the floating gate and which are insulated from the floating gate and semiconductor substrate;

a first capacitance (no number, defined by a conductor/insulator/conductor structure of the semiconducting semiconductor substrate/insulating tunneling gate insulator/floating gate) between the semiconductor substrate and floating gate;

a second capacitance (no number, defined by a conductor/insulator/conductor structure) between the first control gate and floating gate;

a third capacitance (no number, defined by a conductor/insulator/conductor structure) between the second control gate and floating gate;

a fourth capacitance (no number, defined by a conductor/insulator/conductor structure) between the first control gate and semiconductor substrate; and

a fifth capacitance (no number, defined by a conductor/insulator/conductor structure) between the second control gate and semiconductor substrate,

wherein the inter-gate insulating film includes first and second portions, the first portion contacts the floating gate, the second portion contacts the lower surface of the first or second control gate, the first portion is an insulating film, and a second portion is a single layer of a silicon oxide film.

However, as noted, the reference teaches that the first portion of the inter-gate insulating film, which first portion insulates the control gate from the floating gate, is an insulating film instead of a stacked film including a silicon nitride film as claimed.

Wang, in also disclosing a nonvolatile semiconductor memory device including a floating gate, a control gate and an inter-gate insulating film insulating the control gate from the floating gate, teaches that the inter-gate insulating film is a stacked film including a silicon nitride film ("ONO"), instead of an insulating film of silicon oxide, to improve the performance of the nonvolatile semiconductor memory device (column 2, lines 10-15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the reference's device such that the first portion (105a) of the inter-gate insulating film, which first portion insulates the control gate from the floating gate, is a stacked film including a silicon nitride film. One would have been motivated to make such a change in view of the teachings in Wang that such a modification results in a better device.

Referring to **claims 40 and 5**, and using the same reference characters, interpretations, and citations as detailed above for claim 1 where applicable, the reference discloses a nonvolatile semiconductor memory device comprising:

a floating gate formed on a semiconductor substrate via a gate insulating film;

diffused layers, as sources or drain regions, which are positioned on opposite sides of the floating gate and which are formed in the semiconductor substrate;

first and second control gates which are formed on the opposite sides of the floating gate and which drive the floating gate; and

an inter-gate insulating film which insulates the first and second control gates from the floating gate and diffused layers;

wherein the inter-gate insulating film includes first and second portions, the first portion contacts the floating gate, the second portion contacts the lower surface of the first or second control gate, the first portion is an insulating film, and a second portion is a single layer of a silicon oxide.

However, as noted, the reference teaches that the first portion of the inter-gate insulating film, which first portion insulates the control gate from the floating gate, is an insulating film instead of a single layer or a stacked film containing aluminum oxide as claimed.

Wang, in also disclosing a nonvolatile semiconductor memory device including a floating gate, a control gate and an inter-gate insulating film insulating the control gate from the floating gate, teaches that the inter-gate insulating film is a stacked film containing aluminum oxide, instead of an insulating film of silicon oxide or instead of a traditional stacked ONO, to further improve the performance and scaling down of the nonvolatile semiconductor memory device (column 3, lines 6-25, for motivation for change; column 4, last paragraph for definition of "high-K dielectric material"; and column 6, Table 1, for a list of high-K dielectric materials).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the reference's device such that the first portion (105a) of the inter-gate insulating film, which first portion insulates the control gate from the floating gate, is a stacked film containing aluminum oxide, which meets the claimed Markush limitation a single layer or a stacked film containing aluminum oxide. One would have been motivated to make

such a change in view of the teachings in Wang that such a modification results in a better device.

Referring to **claim 2**, the '855 reference further discloses that the inter-gate insulating film (105a/102) contacts opposite (lower) side walls of the floating gate (FG) and lower surfaces of the first and second control gates (CG 103), and the first and second control gates are disposed opposite to the diffused layers (SD).

Referring to **claim 3**, the '855 reference further discloses that a thickness of the second portion (102) is larger than that of the first portion (105a, column 4, lines 43-50, and note that 105a is a portion of 105, as the labels suggest).

## *Allowable Subject Matter*

8. Claims 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a nonvolatile semiconductor memory device having all limitations as in claim 6, characterized in that conductive materials are formed in first and second trenches formed in insulating materials, which are disposed on opposite side surfaces of the floating gate and opposite the diffused layers and which insulate adjacent memory cells, and that the conductive

materials in the first and second trenches constitute said first and second control gates and connect the first and second control gates of adjacent cells.

***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
August 24, 2005